AMENDMENTS TO THE CLAIMS

This Listing of Claims will replace all prior versions, and listings of claims in the Application.

Listing of Claims:

Claim 1 (Currently amended): A circuit system for data transmission between LPC devices, comprising:

a first LPC bus connected to a first LPC device;

a second LPC bus connected to a second LPC device; and,

an LPC host controller including an address register for storing a target address, said LPC host controller being operable to initiate concurrently a first bus access cycle on said first LPC bus and a second bus access cycle on said second LPC bus, said LPC host controller being further operable to initiate said second access cycle upon said target address matching an address on said second LPC bus, said LPC host controller being configured to terminate said first bus access cycle only after said second bus access cycle is terminated.

Claim 2 (Cancelled).

Claim 3 (Previously presented): The circuit system as recited in claim 1, wherein said first LPC device is a master LPC device and said second LPC device is a slave LPC device.

Claim 4 (Cancelled).

Claim 5 (Original): The circuit system as recited in claim 1, wherein said first LPC bus and said second LPC bus are connected to a plurality of LPC devices, respectively.

Claim 6 (Currently amended): A method for data transmission between LPC devices, comprising the steps of:

providing an LPC host controller with an address register for storing a target address;

initiating a first bus access cycle on a first LPC bus by said LPC host controller;

transmitting over said first LPC bus by a first LPC device coupled thereto a request to said LPC host controller for a transaction with a second LPC device coupled to a second LPC bus;

storing an address of a data location on said second LPC device in said address register as said target address;

inserting a plurality of wait states in said first bus access cycle to place said first LPC bus in a wait state after said request is received by said LPC host controller;

initiating a second bus access cycle on said second LPC bus by said LPC host controller concurrently while said first LPC bus is in said wait state; and,

accessing by said LPC host controller said data location over said second LPC bus.

Claim 7 (Previously presented): The method as recited in claim 6 including the steps of:

setting said transaction to be a data read from said second LPC device;

transferring said data from said second LPC device to said LPC host controller over said second LPC bus;

terminating said bus access cycle on said second LPC bus;

terminating said wait state inserting step after said bus access cycle on said second LPC bus is terminated;

transferring said data from said LPC host controller to said first LPC device over said first LPC bus; and,

terminating said bus access cycle on said first LPC bus after said LPC host controller transfers said data to said first LPC device.

Claim 8 (Cancelled).

Claim 9 (Previously presented): The method as recited in claim 6 further including the steps of:

setting said transaction to be a data write to said second LPC device;

transferring said data from said first LPC device to said LPC host controller over said first LPC bus;

transferring said data from said LPC host controller to said first LPC device over said second LPC bus; and,

terminating said bus access cycle on said second LPC bus;

terminating said wait state inserting step after said bus access cycle on said second LPC bus is terminated;

terminating said bus access cycle on said first LPC bus after said LPC host controller transfers said data to said second LPC device.

Claim 10 (Cancelled).

Claim 11 (Currently amended): A circuit system for data transmission between LPC devices, comprising:

an LPC bus;

a master LPC device connected to said LPC bus, said master LPC device including an address register ~~for storing~~ operable to persistently store a target address;

at least one slave LPC device connected to said LPC bus; and

an LPC host controller including an address register ~~for storing~~ operable to persistently store said target address, said LPC host controller being operable to initiate a data transfer cycle on said LPC bus, said data transfer cycle ~~including both~~ being a concatenation of a first bus access cycle for LPC bus access by said master LPC device and ~~by~~ a second bus access cycle for LPC bus access by one of said at least one slave LPC device.

Claim 12 (Previously presented): The circuit system as recited in claim 11, wherein each of said at least one slave LPC device includes an address register for storing said target address.

Claim 13 (Currently amended): A method for data transmission between LPC devices, comprising the steps of:

providing an LPC master device with an address register ~~for storing~~ operable to store a target address persistently over at least two bus access cycles on an LPC bus;

initiating a first bus access cycle on ~~an~~ said LPC bus by said LPC host controller;

transmitting a request for a transaction over said LPC bus from said master LPC device to said LPC host controller, said transaction specifying a transfer of first data between said master LPC device and a slave LPC device;

transferring second data between said LPC host controller and master LPC device during said first bus access cycle;

storing an address of a data location on said slave LPC device in said address register of said master LPC device as said target address;

initiating a second bus access cycle on said LPC bus by said LPC host controller;

transferring said first data between said LPC host controller and said slave LPC device during said second bus access cycle.

Claim 14 (Previously presented): The method as recited in claim 13 further including the steps of:

setting said transaction to be a data read from said slave LPC device; and,

setting said second data to an arbitrary data value.

Claim 15 (Cancelled).

Claim 16 (Currently amended): The method as recited in claim 14, further comprising the steps of:

providing said LPC host controller with an address register ~~for storing~~ operable to persistently store said target address; and,

storing said address of said data location in said address register of said LPC host controller after said LPC host controller has received said transaction request from said master LPC device.

Claim 17 (Currently amended): The method as recited in claim 16, further comprising the steps of:

transferring said first data from said slave LPC device to said LPC host controller; and

monitoring said LPC bus at said master LPC device for data transferred from said slave LPC device; and,

accepting at said master LPC device said data transferred from said at least one slave LPC device as said first data if a source address thereof is equivalent to said target address stored in said address register of said master LPC device.

Claim 18 (Previously presented): The method as recited in claim 13 further including the steps of:

setting said transaction to be a data write to said slave LPC device; and,

setting said second data to equal said first data.